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Traditional bulk silicon encounters performance limitations in shrinking CMOS transistor feature size to 65nm. But, through the use of silicon-germanium, strained silicon, and silicon-on-insulator and, ultimately, germanium-on-insulator technology, the life of silicon substrates could be stretched as far as the 22nm generation.

Stretching silicon's lifespan

According to the *International Technology Roadmap for Semiconductors*, as CMOS transistor dimensions shrink beyond the 65nm generation to 45nm, bulk silicon will encounter fundamental limits of channel mobility and gate leakage current. Indeed, the 130nm and 90nm generations already partly rely on engineered silicon substrates.

Silicon on insulator (SOI) introduces a buried layer of insulating oxide between the bulk and the upper surface of the silicon wafer. This increases electrical isolation and reduces parasitic junction capacitance between device and substrate. That decreases transistor delay time, enabling higher-speed digital ICs, and increasing drive currents, while lowering noise and power consumption (by up to a factor of four).

In 2003 SOI represented just 2.5% of total silicon revenues but up to 10% for leading-edge technology nodes, and has a compound annual growth rate three to four times that of silicon. For 65nm technology, SOI adoption is expected to increase dramatically for high-end microprocessor and logic ICs.

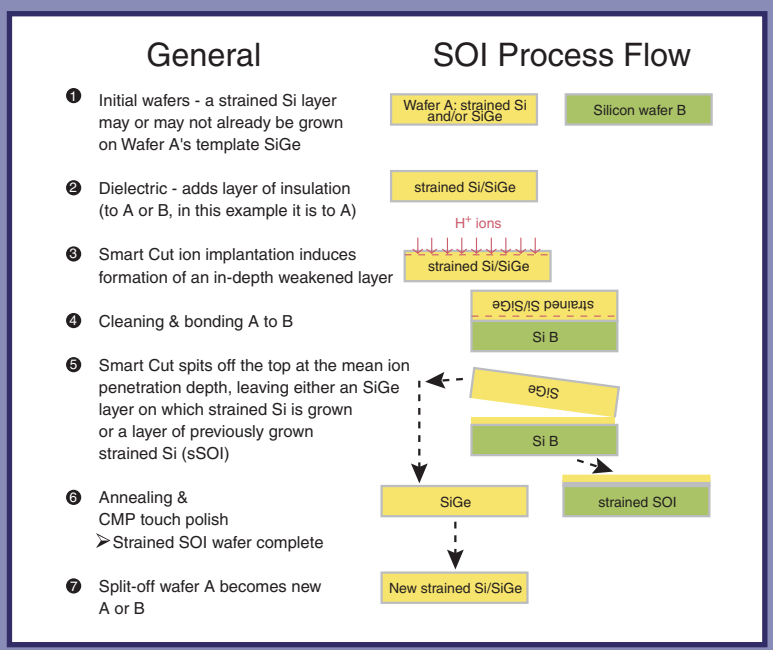

Figure 1. A SiGe "virtual" substrate induces strain in silicon grown on top.

France's Soitec was founded in 1992 as the first company devoted to volume SOI material manufacturing, and claims that its Smart Cut wafers have 90% share of the thin-film SOI market (including 10% through licensee Shin-Etsu Handotai). Its June quarter saw record sales, up 68% on a year ago, boosted by demand for 300mm SOI wafers, which are being introduced by IBM, Sony, and AMD in 2005. In addition to Soitec's Bernin I 4-8" wafer plant, Bernin II has a capacity of 120,000 300mm wafers per year (rising ultimately to 720,000).

Analysts forecast that, by 2005, 45% of SOI demand will switch to 300mm, comprising nearly 50% of 300mm substrates consumed by 2009.

Strained silicon

Device performance can be further improved, without shrinks and related capital cost increase, by epitaxially depositing silicon-germanium (SiGe). Due to a lattice constant mismatch of 4.2% between Si (5.431Å) and Ge (5.657Å), in $Si1_{-x}Ge_x$ (where $o<_x<_l$) the distance between silicon atoms is stretched. Such tensile strain increases the mobility of charge carriers in a SiGe-based transistor, speeding devices.

A strain-relaxed $Si1_{-x}Ge_x$ graded buffer layer on silicon can also provide a SiGe 'virtual' substrate for epitaxy of silicon, with in-built strain (see Figure 1), enabling a higher-mobility channel layer for 65-45nm CMOS transistors.

UK epiwafer foundry IQE plc aims to be the first licensee of Salem, NH-based, AmberWave Systems' strained-silicon technology for 150 and 200mm wafers, reckoning on extending the life cycle of a fab by two to three years.

Strained SOI

The high speed of strained silicon can be combined with the low-power benefits of SOI, resulting in strained SOI wafers for 65-45nm CMOS from 2005:

(1) In SiGe-on-insulator (SGOI), a relaxed SiGe layer is transferred onto an oxidised silicon wafer, followed by removal of the donor substrate. Strained silicon can be deposited either before transfer (before the SiGe layer is deposited and on top of a graded $Si_{1-x}Ge_x$ buffer layer, which is removed after transfer) or after transfer (on to what has become a silicon-germanium on insulator substrate), forming a substrate for epitaxy of strained silicon (see Figure 2a).

However, the quality of the SiGe and buried oxide (BOX) layers is a concern, causing material and process integration challenges. In addition, Ge segregation during high-temperature annealing also limits the maximum Ge composition to a low value. A major concern about the manufacturability is the high level of crystal defects in the strained Si layer, typically due to the epi technique used to grow the SiGe templates.

(2) In strained silicon directly-on-insulator (SSDOI) - or strained silicon-on-insulator (s-SOI) - a thin layer of strained silicon is epitaxially deposited on a relaxed SiGe buffer layer, *before* an oxide layer is formed. After hydrogen implantation into the SiGe, flipping and bonding of the wafer to a handle substrate, and high-temperature splitting away of the bulk silicon, the remaining SiGe is removed, leaving SiGe-free strained SOI (see Fig 2b).

Processes have been demonstrated by IBM, Massachusetts Institute of Technology and AmberWave Systems. In September 2003 IBM claimed fabrication of the first transistors using ultra-thin SSDOI, confirmed electron and hole mobility enhancements in MOSFETs, and fabricated sub-60nm FETs.

Commercial SGOI and sSOI

Extending a previous collaboration on Soitec's 300mm Unibond SOI wafers that used Advance 400 Series vertical furnaces from Netherlands-based ASM International, in May 2003 a joint strained SOI partnership programme was initiated that combines Soitec's Smart Cut SOI technology with strained silicon epi deposition using ASM's Epsilon 3000 reactor. This led in July 2003 to industry-first samples of first-generation strained SOI wafers for 65nm technology.

Soitec's first strained SOI product consists of a 200mm fully relaxed SGOI template substrate, incorporating 20% Ge (with or without growth of the final strained silicon layer). The wafers can be tailored for both partially depleted and fully depleted device architectures, offering strain reproducibility in silicon layers as thin as 15nm.

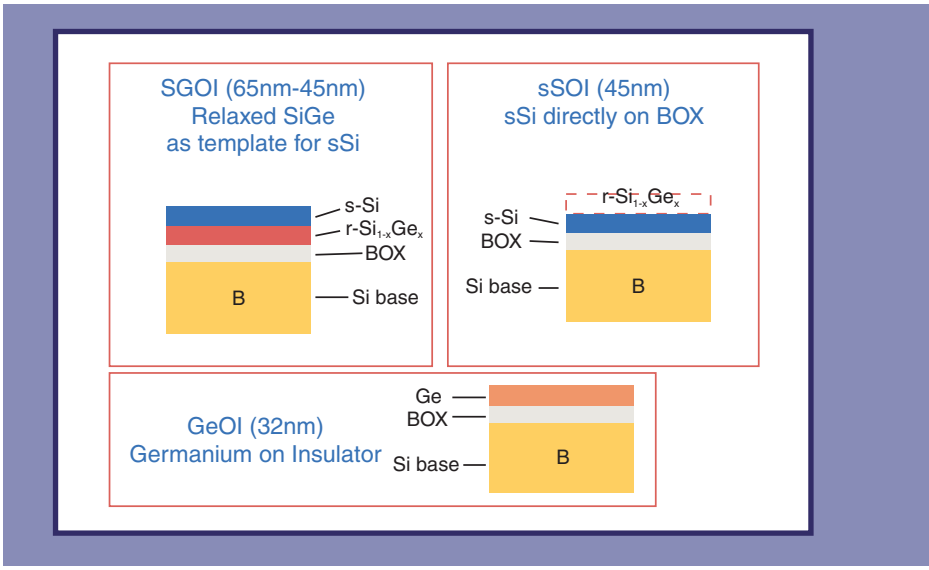

Figure 2. Structure for a) SiGe-on-insulator (SGOI), (b) strained silicon-on-insulator (sSOI), and (c) germanium-on-insulator (GeOI).

To enable early sampling, concurrent with the development of the epi modules a 'virtual fab' operation processes wafers at both companies, enabling fine-tuning of the epi processes to optimise substrate performance, boost productivity and maximise cost efficiency, before Sooitec announced last December that it was installing epi equipment in its pilot line and a full SGOI and s-SOI manufacturing line at its new 300mm Bernin II plant.

SGOI early production was due to start in Q4/2004. "The ability to perform the epitaxy process in our own production facility will help ensure that we can rapidly deliver volume quantities of high-quality strained SOI wafers," says president and CEO André Auberton-Herve. Full capacity will be more than 60,000 200mm-equivalent wafer starts per year.

Using an ASM A412 vertical furnace and a low-temperature-enhanced Epsilon 3200 reactor, this July saw the industry's first 300mm strained silicon substrates, the first high-quality sSOI with wafer-level strain rather than local strain, reducing the high level of crystal defects to nearer to that of standard SOI and bulk silicon.

"Customer and internal evaluations show that the strain of s-SOI is very robust, surviving the typical thermal budgets of 65nm CMOS processes," claims CTO Carlos Mazure. "Strained SOI appears to offer the greatest potential for improving the performance of ICs with 65nm and below design rules", adds Auberton-Hervé.

Subsequent generations of strained silicon will include SGOI with higher Ge content, strained

SOI without the SiGe template layer (s-SOI), and germanium-on-insulator (GeOI) - see Figure 3.

Current relaxed SiGe-based strained silicon and s-SOI are based on biaxial wafer-level strain (uniform over the substrate's device fabrication surface).

But biaxial strain suffers from high defect levels and germanium inter-diffusion, leading to mobility degradation at high effective gate electric fields (~1MV/cm) and much lower efficiency in boosting PMOS transistor performance, contrast in uniaxial strain, where the device silicon film is strained in a single direction on the crystal surface to enhance the mobility.

Uniaxial vs biaxial strain

Benefits of uniaxial strain at the local, transistor level have been demonstrated by chip makers including Intel, TSMC and Texas Instruments. Local strain uses micron-scale epi deposition to strain selected transistor regions. Intel's 90nm technology is first to implement a uniaxial strained silicon process with different stress techniques on the NMOS and PMOS transistors.

Dr Scott Thompson, University of Florida associate professor and former director of Intel's 90nm Logic Technology and Strained Silicon Programme, adds: "Uniaxial strain is now being recognized as the preferred strain type for deep-submicron device applications, and its local variant has displaced global biaxial strain as the mobility enhancer of choice".

Wafer-level vs local strain

This August Silicon Genesis Corp said it had developed 'Next-Generation Strain', the first *wafer-level* uniaxial strained substrates. President and CEO Francois J Henley says it can "significantly enhance mobility over SiGe-based biaxial strain." It is also compatible with local straining techniques and is therefore additive, boosting transistor performance further. SiGen's process can achieve stress of over 1GPa in a uniaxially strained silicon layer, either on top of a buried oxide (s-SOI) or as a bulk Si wafer (s-Si/bulk).

Low-temperature processing yields low defect levels. It can be directly integrated on silicon as an 'epi-like' strained bulk wafer or on insulator as s-SOI. Production costs are expected to be significantly lower than biaxial technologies by avoiding growing and relaxing thick SiGe layers steps.

"Aavailability of a wafer-level uniaxially strained substrate works with these existing approaches to substantially improve total transistor performance and has scaling advantages over local strain at the 45nm node and beyond," Henley adds.

In line with its new IP business model strategy, SiGen is pursuing development and commercialisation with partners.

Towards 32-22nm: GeOI

In 2003 Belgian microelectronics research centre IMEC launched two industrial affiliation programmes (IIAPs) targeting sub-45nm processes:

(1) "Implementation of high-mobility layers and advanced source/drain engineering solutions in scaled planar devices" (ie. strained silicon in a MOS transistor's channel): IMEC has fabricated strained silicon transistors on thin (sub-200nm) strain-relaxed SiGe buffers that show record hole mobility in hetero-pMOS with strained SiGe.

(2) Germanium-based CMOS transistors compatible with silicon process lines (200mm, migrating to 300mm). In Ge channels, carrier mobilities for both electrons and holes are higher than silicon's (by two and four times, respectively) tripling transistor switching speed.

IMEC has examined deposition on Ge of MOS gates, comprising TaN metal and HfO_2 high-k dielectric (a promising replacement for SiO_2 in silicon CMOS but also overcoming the unstable nature of germanium oxide, allowing aggressive scaling of the equivalent oxide thickness). Wet treatment with hydrofluoric acid, followed by an NH_3 anneal at 600°C created a smooth Ge-HfO_2 interfacial layer to avoid Ge diffusion. Ge's lower-temperature activation of dopants (implantated boron for n-type and arsenic for p-type) enabled the formation of shallow junctions.

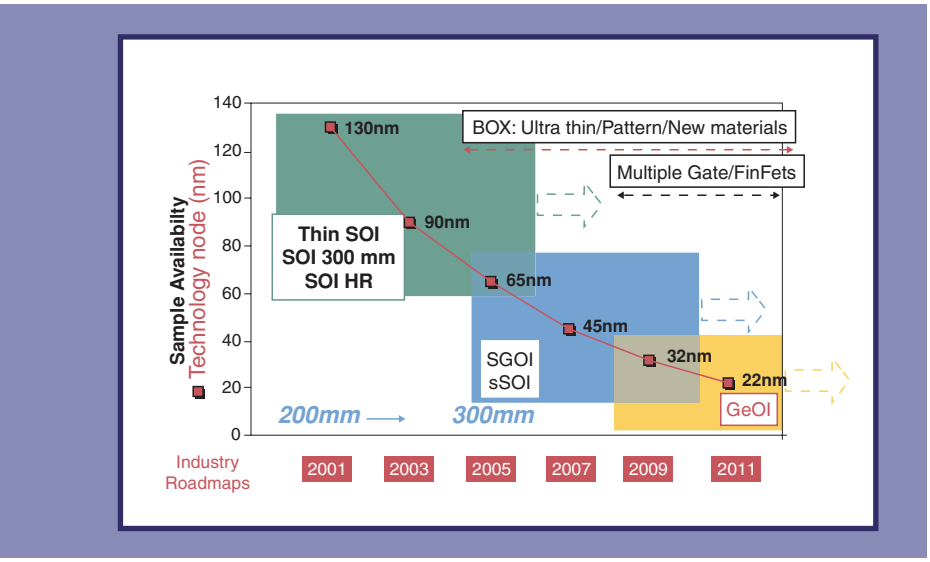

Figure 3. SOITEC's roadmap for SiGe-on-insulator, strained silicon-on-insulator, and germanium-on-insulator.

To avoid the need for bulk Ge substrates, September 2003 saw collaboration on the fabrication of germanium-on-insulator (GeOI) substrates, using Soitec's Smart Cut process to transfer a thin Ge layer from Umicore's Ge bulk wafers on to an insulating oxide layer on a silicon substrate. In March Soitech agreed to combine Smart Cut expertise with the deposition capabilities of Applied Materials Inc's Centura RP Epi system, which can deposit virtually any Ge/Si combination up to 100% Ge.

Subsequently, IMEC's 200mm silicon prototyping line has fabricated a transistor device with an isolation structure and a directly etched gate stack. Extensions were implanted and spacers formed prior to source/drain implantation.

Marc Meuris, director of the germanium CMOS device programme,says that to achieve the higher yield and reliability required for ULSI circuits, low-defect substrates need to be developed.

In March 2003, Silicon Genesis detailed its development of GeOI. SiGen's layer transfer process is suited to creating heterogeneous layered structures, since low processing temperatures minimise adverse temperature affects on materials such as germanium, and allow layer transfer of materials other than silicon to various substrates.

GeOI is used by IBM to develop Ge photodetectors integrated on silicon for on-chip optical communications. Ge's close match in lattice parameter with GaAs could offer the missing link vital for cost-effective on-chip integration of active optical components.

SOI: bonded vs SIMOX

In the manufacture of SOI wafers, a buried oxide can be fabricated by separation by implanted oxygen (SIMOX) or by wafer bonding. SIMOX involves oxygen ion implantation into the wafer's surface, followed by a high-temperature anneal, then thermal oxidation.

Ideal for bulk silicon, SIMOX is not so successful for strained SiGe-on-insulator (SGOI) with Ge content above 30% and cannot handle strained silicon directly on insulator (SSDOI). But wafer bonding does allow SGOI with any Ge content, as well as SSDOI.

In January, silicon wafer maker MEMC Electronic Materials Inc licensed NanoTec layertransfer SOI technology and bought room-temperature controlled cleaving and integrated Plasma Activation bonding tools from Silicon Genesis Corp. "We had previously considered bonded and SIMOX technologies to be viable options," said CEO Nabeel Gareeb. However, non-contact wafer smoothing yields improved SOI layer thickness uniformity (required for fully depleted SOI < 65nm) and gave flexible derivative developiment

Believing dedicated wafer manufacturers are best-positioned to meet demand, in July, SIMOX-focused Ibis Technology Corp terminated volume SOI wafer manufacture to focus on supplying SOI ion implanters.

This February Wacker Chemie's Siltronicdivision,licensed Soitec's Smart Cut technology (to produce bonded SOI wafers in second-half, 2005) and agreed a joint programme to accelerate development of strained SOI.

"With acceleration of new technology nodes, and the resulting industry shift to the advanced materials for device performance and low power consumption, SOI has become a critical, enabling technology," said CEO Wilhelm Sittenthaler.

The 50th International Electronic Device Meeting

This historic conference, which traditionally always produces a cornucopia of ingenious devices, from which the key developing trends emerge, is held this year in San Francisco, 13-15 Decem-ber.

Extending silicon can be found throughout the entire meeting, but two session are specifically devoted to strained Si & CMOS devices and one to SiGe HBTs

IBM's redoubtable T J Watson Centre researchers have work on *Selectively formed, high mobility strained Ge PMOSFETs for high performance CMOS* and *SiGe HBT technology with gate delay below 3.3ps* as well as work on *Performance comparison and channel length scaling of strained Si FETs on SGOI.*

From Taiwan, TSMC researchers present on *Low power device technology with SiGe channel, HfSiOn and Poly-Si gate*, while the National Chiao Tung University and Yun-Lin Polytechnic Institute contribute *Three dimensional GOI CMOSFETs with novel IrO2 (Hf) dual gates and high-k dielectric on 1P6M-0.18mm CMOS."*

Japan papers include Toshiba Corporation and Sony work on *The parasitic resistance and silicon layer thickness scaling for strained silicon MOSFETs on relaxed $Si1_{-x}Ge_x$ virtual substrate.*

Toshiba Ceramics, Komatsu Electronic Materials and MIRAI-AIST look at *Performance enhancement of partially, and fully-depleted strained SOI MOSFETs and characterisation of strained-Si device parameters.*

And from IHP Frankfurt, Germany comes *Integration of High Performance SiGe:C HBTs with thin-film SOI CMOS* and Infineon's work is on *3.3ps SiGe bioplar technology.*